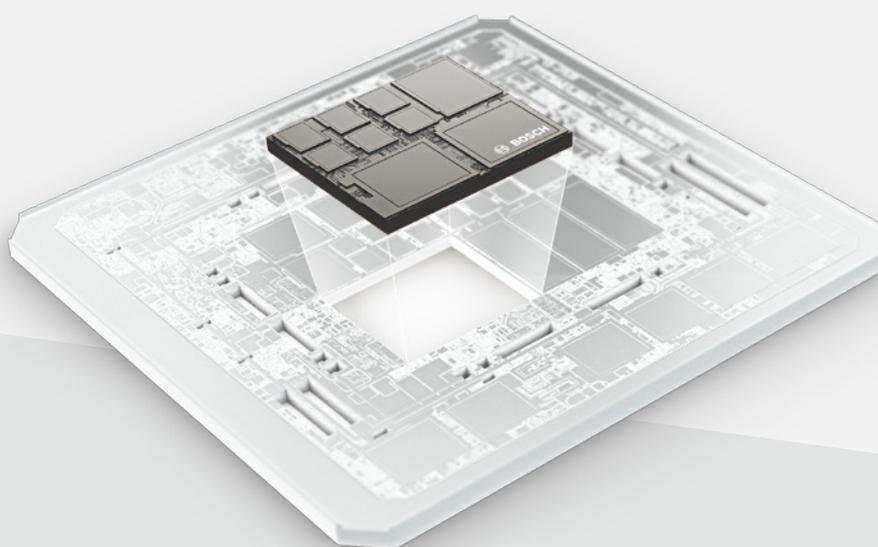# Automotive and industrial control units

M_CAN protocol controller IP for CAN (FD)

BOSCH
Invented for life

PRODUCT BENEFITS

- ▶ Support of Classical CAN and CAN FD up to 64 byte according to ISO 11898-1:2015
- ▶ Support of TTCAN (Time-Triggered CAN) according to ISO 11898-4
- ▶ Multiple M_CAN modules can access one shared memory
- ▶ Smart message handling reduces CPU load
- ▶ TTCAN for real-time applications
- ▶ Connectable to customer-specific Host CPUs with 8/16/32-bit generic CPU interface

up to
64 byte

payload for faster transmission of large data fields

secure communication

with bitrates above 1 Mbit/s

TASK
The M_CAN protocol controller IP enables event- and time-triggered communication according to ISO 11898-1:2015 and ISO 11898-4.

FUNCTION
The IP module is integrated into a microcontroller, a dedicated ASIC, or FPGA and ensures the protocol conform handling of data transfer via CAN bus. It filters messages received from the CAN bus and sorts transmit messages according to their priority and thereby reduces interrupt load.

VARIANTS
The IP module is available as M_CAN and M_TTCAN for integration into microcontrollers, ASICs, or FPGAs.

M_CAN IP MODULE FOR ASIC DESIGN

M_CAN	31.0 k gates
Message RAM	max. 17 kB/M_CAN instance
Deliverables for ASIC design	VHDL source code, VHDL test bench environment, documentation, conformance test report

M_CAN IP MODULE FOR FPGA DESIGN

Altera (Cyclone III)	8,200 logic elements
Xilinx (Spartan 6)	5,850 LUTs
Message RAM	max. 17 kB/M_CAN instance
Deliverables for FPGA design	encrypted VHDL source code, VHDL source code of an example system design with RAM and an example arbiter instance, documentation, conformance test report, programming examples for fast start up