GTM
system integration aspects in semiconductor and ECU

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GTM system integration aspects in semiconductor and ECU
Introduction: Challenge µController Platform development

- Initial Situation
  - Individual requirements coming from a large number of OEMs
  - Great variance of requirements (2-wheeler to 8 Cylinder Diesel or Gasoline direct injection)
  - Different Engine Control Units like gasoline, diesel, hydrogen and vehicle control Units

- Solution
  - Highly scalable µC family concept which defines Standard functionality mandatory
    - across different µC sizes
    - compatible packages
    - pin-out
    - µC generations

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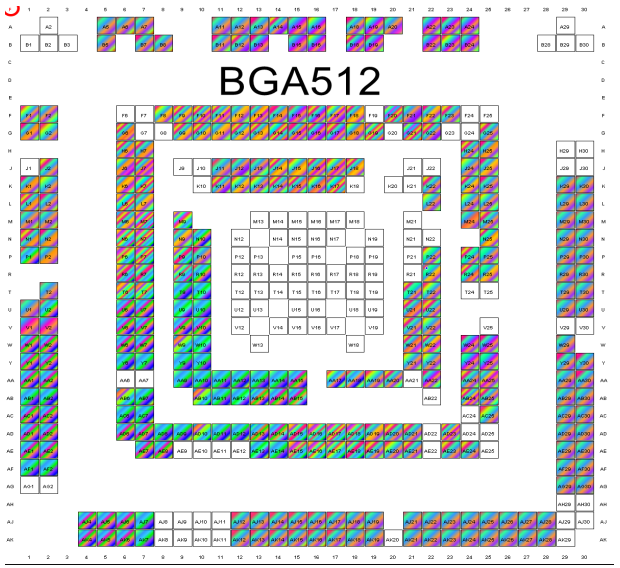
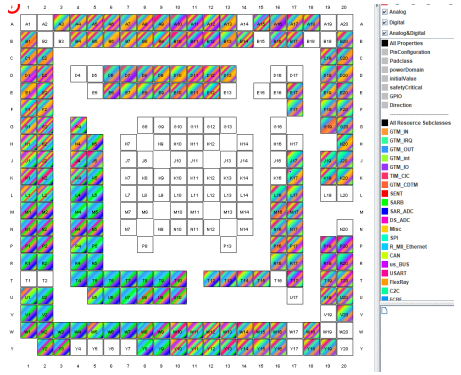
Definition µC Family concept

- Example BGA Family Platform across controller Generations:
- **Two standard BGA packages**
  - BGA512 with maximum number of IO Pins
  - BGA292 compatible to the inner ball rows of the BGA516
- **Different performance classes**
  - Smaller µC compatible in the same package variants
- **Different Controller Generations**
  - New µC Generation backward compatible to former one
- **Different Supplier**
  - Multiple compatible supplier available for each µC generation





Device	Package	
DEV5	BGA512	BGA292
DEV4	BGA512	BGA292
DEV3		BGA292

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µC Family concept

- Advantages Family Concept:
  - Scalable combined layout feasible
    - one layout with a BGA512 footprint could support BGA292 (assembly variants possible)
  - µC size which suits to project requirements
  - uniform Base-SW

- How did we get there
  - uniform sourcing of the various µC suppliers via standard request form
    - Equal definition of
      - electrical and functional pin behavior (e.g., hysteresis, voltage level, driver strength,…)
      - IO-Multiplexing (MUXing) for all internal modules
      - same GTM–REV in one µC generation to assure same functionality

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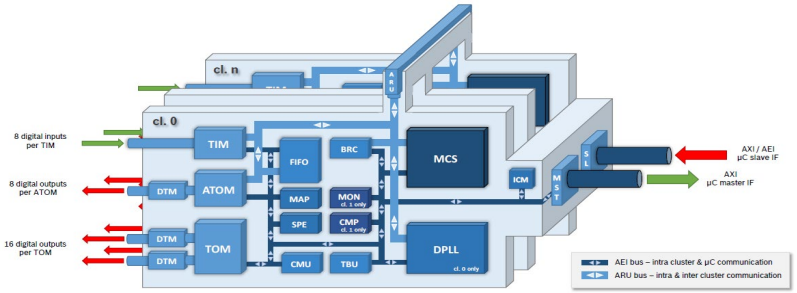
How the GTM supports the µC Family concept



- modular and easily scalable
  - Timer functions are grouped in modular clusters
  - Content of the GTM-IP for a new µController defined during the sourcing of the device
    - during design phase, chip manufacturer orders tailored GTM-IPs via AE standard form
- Bosch AE guarantees backward compability of basic timer functionality
  - Features in new Generation must not affect the old ones
    - if small SW adaptations are required, this must be explicitly pointed out
- Integration of the GTM-IP into the devices
  - New GTM functionality (e.g., IO-Muxing TIO IN/OUT in the GTM V4.x) must be introduced **equal** across chip vendors

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Advantages of the unified GTM module

- all real time functions could be combined standardized into the module
  - Low risk and rework for the critical real time applications when change to new µC
  - Reuse of complex MCS real time libraries
- HW-platform validation in new devices with limited effort
- Validated GTM ERRATA workaround reusable in each Family µC
- Fast introduction of a new µC Generation
  - Projects could start with legacy functionality
  - New functions (like TIOs) could be introduced after validation and available SW support

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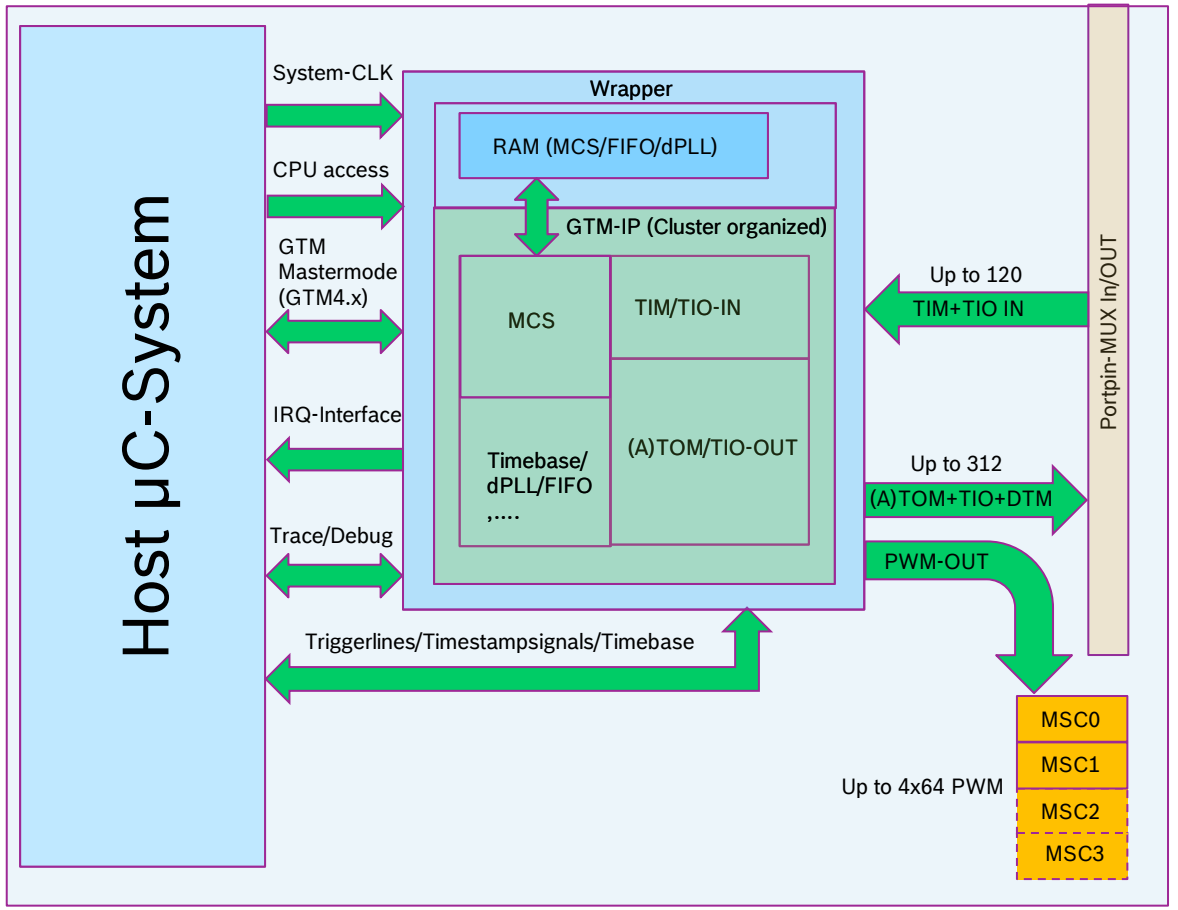
Integration of the GTM-IP into the µC

- Interconnections of the GTM



GTM-Ordersheet (example)

	Total		Cluster 0	Cluster 1	Cluster 2	Cluster 3	Cluster 4	Cluster 5	Cluster 6	Cluster 7	Cluster 8	Cluster 9	Clu
Cluster & Cluster Speed/Clock Divider	10	39	1:1 & 2:1	1:1 & 2:1	1:1 & 2:1	1:1 & 2:1	1:1 & 2:1	1:1 & 2:1	1:1 & 2:1	1:1 & 2:1	1:1 & 2:1	1:1 & 2:1	not
Generate Clock-Enables	internal												
CMU - Clock Management Unit	yes	14	yes										
TBU - Time Base Unit	yes		yes										
TBU Channels	3	3	ch. 0 - 2										
TBU Channel 3 (special channel)	no	0											
TIM - Timer Input Module	7	482	yes	yes	yes	yes	yes	yes	yes				
TIM Channels	56		8	8	8	8	8	8	8				
TOM - Timer Output Module	5	244	yes	yes	yes	yes	yes						
TOM Channels	80		16	16	16	16	16						
HighRes Supported Channels		0	no	no	no	no	no						
ATOM - ARU-Connected TOM	10	590	yes	yes	yes	yes	yes	yes	yes	yes	yes	yes	
ATOM Channels	80		8	8	8	8	8	8	8	8	8	8	
HighRes Supported Channels		0	no	no	no	no	no	no	no	no	no	no	
TIO - Timer Input/Output Module													
TIO Module Type	TIOp8	238											
TIO Modules (cluster with TIO)	8		no	yes	yes	yes	yes	no	yes	yes	yes	yes	
TIO Channels	64			8	8	8	8		8	8	8	8	
DTM - Dead-Time Module(s)	22	92											
Clusters with DTM after TOM ch. 0..7	4		DTM[0,1]	DTM[0,1]	DTM[0,1]	DTM[0,1]							
Clusters with DTM after TOM ch. 8..15	0												
Clusters with DTM after ATOM ch. 0..7	7		DTM[4,5]	DTM[4,5]	DTM[4,5]	DTM[4,5]	DTM[4,5]	DTM[4,5]	DTM[4,5]				
Clusters with DTM after TIO ch. 0..7	0												
Clusters with DTM after TIO ch. 8..15	0												
Clusters with DTM after TIO ch. 16..23	0												
MCS - Multi-Channel-Sequencer	10	1.587	yes	yes	yes	yes	yes	yes	yes	yes	yes	yes	
MCS channels	80		8	8	8	8	8	8	8	8	8	8	
MCS Memory	180 kByte												
MCFG - Memory Config	no	0											
Full/Half RAM 1 Option	half												
MCS RAM0 Config (kByte)	120 kByte		16	16	16	16	16	8	8	8	8	8	
MCS RAM1 Config (kByte)	60 kByte		8	8	8	8	8	4	4	4	4	4	
DPLL - Digital PLL	yes	125	yes										
PMT Channels	32		32										
DPLL RAM 1a Config	128x24 bit		128x24 bit										
DPLL RAM 1b Config	384x24 bit		384x24 bit										
DPLL RAM 2	4096x24 bit		4096x24 bit										
ARU - Advanced Rounting Unit	yes	26	yes										
ARU Channels	2												
BRC - Broadcast Unit	yes	20	yes										
BRC Channels Out	12		12										
FIFO	3	121	1x	1x	1x								
FIFO PSM Channels	3x 8 ch		8 ch	8 ch	8 ch								

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Port Assignment Challenge

- Bootleneck up to >700 pin functions divided into 330 I/O pins
  - Several digital and analog modules integrated
  - Each project needs tailored Port Assignment
  - Especially critical for the GTM timer with very high number of In/OUT functions
  - Flexibility needed

Example DEV5

Module	Pincount
Analog Pins	100
Ethernet	25
FlexRay	4
20 CAN	40
10 SPI	80
4 MSC (µS Bus)	28
10 UART	20
4 PSI5	8
30 SENT	30
GTM TIM/TIO/(A)TOM/DTM	430
Total functions	765
BGA512 Available IO	330
BGA292 Available IO	200

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I/O Integration of the GTM into the µC: Pin-Multiplexing

- Each IO pin offers a variety of optional signals like CAN, SPI,… and GTM signals
- To guarantee availability every TIM/TIO/(A)TOM Timer cell is connected
  - In various combinations
  - Multiple times
  - On different pins

Pin	GTM IN			GTM OUT						CAN	CAN	FlexRay	USART	SPI	µs-Bus	SENT	PSI5	I2C	ADC
G6	TIM0_0	TIM1_0		TOM0_8	TOM1_8	TOM0_0	ATOM0_0	ATOM1_0	ATOM0_5_N	CAN00_TX		FlexRay0_TXD0A	TXD2	SLSO31					
H7	TIM0_1	TIM1_1		TOM0_9	TOM1_9	TOM0_1	ATOM0_1	ATOM1_1	ATOM0_6_N	CAN00_RX		FlexRay0_RXD0A2	RXD2	SLSO32					
H6	TIM0_2	TIM1_2		TOM0_10	TOM1_10	TOM0_2	ATOM0_2	ATOM1_2	ATOM0_7_N	CAN02_TX		FlexRay0_TXD0B	TXD1	SLSO33		SENT14	PSI-TX0		
J7	TIM0_3	TIM1_3		TOM0_11	TOM1_11	TOM0_3	ATOM0_3	ATOM1_3	ATOM0_4_N	CAN02_RX		FlexRay0_RXD0B2	RXD1	SLSO34	MSC1_SDI1	SENT13	PSI-RX0		
J6	TIM0_4	TIM1_4		TOM0_12	TOM1_12	TOM0_1_N	ATOM0_4	ATOM1_4	ATOM0_1_N	CAN0_ECTT1	CAN11_RX	FlexRay0_TXEN0A	CLK2	SLSO30		SENT12		SDA0	
K7	TIM0_5	TIM1_5		TOM0_13	TOM1_13	TOM0_2_N	ATOM0_5	ATOM1_5	ATOM0_2_N	CAN0_ECTT2	CAN11_TX	FlexRay0_TXEN0B		MRST3		SENT3		SCL0	
K6	TIM0_6	TIM1_6	TIM3_0	TOM0_14	TOM1_14	TOM0_3_N	ATOM0_6	ATOM1_6	ATOM0_3_N					MTSR3		SENT2			
L7	TIM0_7	TIM1_7	TIM3_1	TOM0_15	TOM1_15	TOM0_0_N	ATOM0_7	ATOM1_7	ATOM0_0_N					SCLK3		SENT1	PSI-RX2		
L6	TIM2_0	TIM3_0	TIM3_2	TOM0_8	TOM1_0	TOM4_4	ATOM0_0	ATOM1_0	ATOM0_5_N					SLSO35		SENT0	PSI-TX2		
M6	TIM2_0	TIM3_0	TIM5_4	TOM0_8	TOM1_0	TOM0_0_N	ATOM0_0	ATOM1_0	ATOM0_5_N		CAN10_TX		TXD3		MSC0_INJ0				
M7	TIM2_1	TIM3_1	TIM5_5	TOM0_9	TOM1_1	TOM0_1_N	ATOM0_1	ATOM1_1	ATOM0_6_N		CAN10_RX		RXD3			SENT0	PSI-RX0		AN61
N6	TIM2_1	TIM3_1	TIM5_6	TOM0_9	TOM1_1	TOM0_2_N	ATOM0_1	ATOM1_1	ATOM0_6_N	CAN03_TX	CAN21_TX			SLSO34		SENT1	PSI-TX0		AN60
N7	TIM2_2	TIM3_2	TIM5_7	TOM0_10	TOM1_2	TOM0_3_N	ATOM0_2	ATOM1_2	ATOM0_7_N	CAN03_RX	CAN21_RX					SENT2			AN59
P6	TIM2_3	TIM3_3	TIM6_4	TOM0_11	TOM1_3		ATOM0_3	ATOM1_3	ATOM0_4_N		CAN11_TX					SENT3			AN58
R7	TIM2_4	TIM3_4	TIM3_0	TOM0_12	TOM1_4	TOM0_1_N	ATOM0_4	ATOM1_4	ATOM0_1_N		CAN11_RX			SLSO33		SENT4	PSI-RX3		AN57

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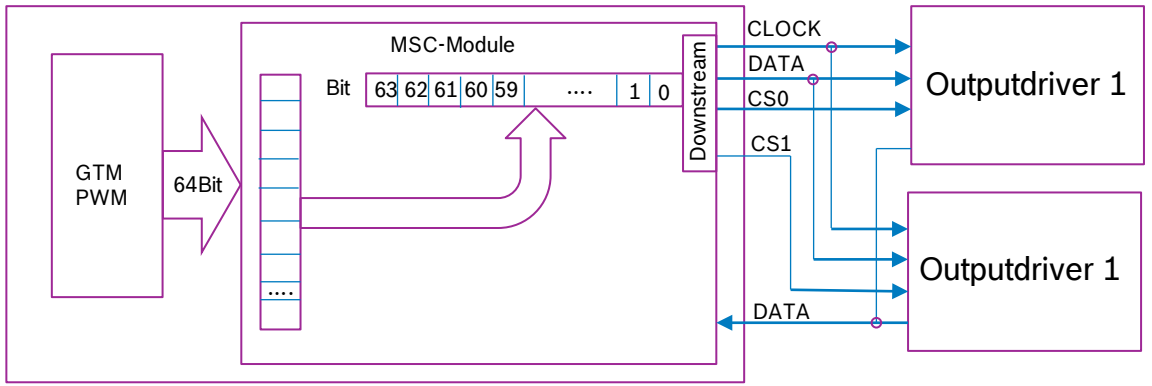
I/O Integration: Virtual OUTPUT Portpins via MicroSecondBus (MSC)

- Every µC offers a set of serial high-speed Buses to connect Output-Driver ASICs
  - Up to 4 MSC Buses (biggest DEV5)
  - Each Bus up to 64 channel for PWM signals
  - For each of the 64Bit variety of GTM Timer OUT (TOM or ATOM) selectable
    - selectable resources compatible across the µC family



Example MSC Select

	MSC0			
MSC-Bit	0 to 15	16 to 31	32 to 47	48 to 63
	TOM0_x	TOM1_x	TOM0_x	TOM0_x
	ATOM0_x	ATOM2_x	TOM1_x	TOM1_x
	ATOM1_x	ATOM3_x	TOM2_x	TOM2_x
	ATOM2_x	ATOM0_x	ATOM0_x	ATOM0_x
	ATOM3_x	ATOM1_x	ATOM1_x	ATOM1_x
	TOM2_8 to TOM2_15	ATOM4_x	ATOM2_x	ATOM2_x
			ATOM3_x	ATOM3_x
			ATOM4_x	ATOM4_x
			TIO1_x	TIO1_x
			TIO2_x	TIO2_x
			TIO3_x	TIO3_x
			TIO4_x	TIO4_x

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I/O Integration: Overview of internal GTM connections

- Support of Engine Position Management with the integrated dPLL
- SAR-ADC and Delta-Sigma ADC
  - Flexible trigger line configuration
  - Timestamping with different timebases
  - Fast comparator (A)TOM Shutoff
  - Direct ADC->MCS Interface for ADC values
- Trigger into other digital modules
- GTM-IRQs into the system
- GTM-MCS Mastermode access into the µC-System (new with GTM 4.x)
  - Support for Multi-Domain usage

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Assignment of µC functions to individual layouts

- Handling of complex µC Pin-Multiplexing done by automated process
  - Following the µC Family approach.
  - Works with a model compatible to different µController
  - Combi model is generated from machine readable IO-MUX descriptions from Chip vendor
  - Deviations from family concept in function and PinMUX **are filtered out**
  - Combi Model could be eighter
    - over different µC Generations (to ensure backward compability)
    - only in the same µC Generation between different vendors for introduction of new feature sets or enhancements
  - Tool considers port assignment relevant µC ERRATAs and rule sets
  - Automated configuration of GTM settings like ADC Trigger, MCS usage, Timer requirements,…

BACKUP

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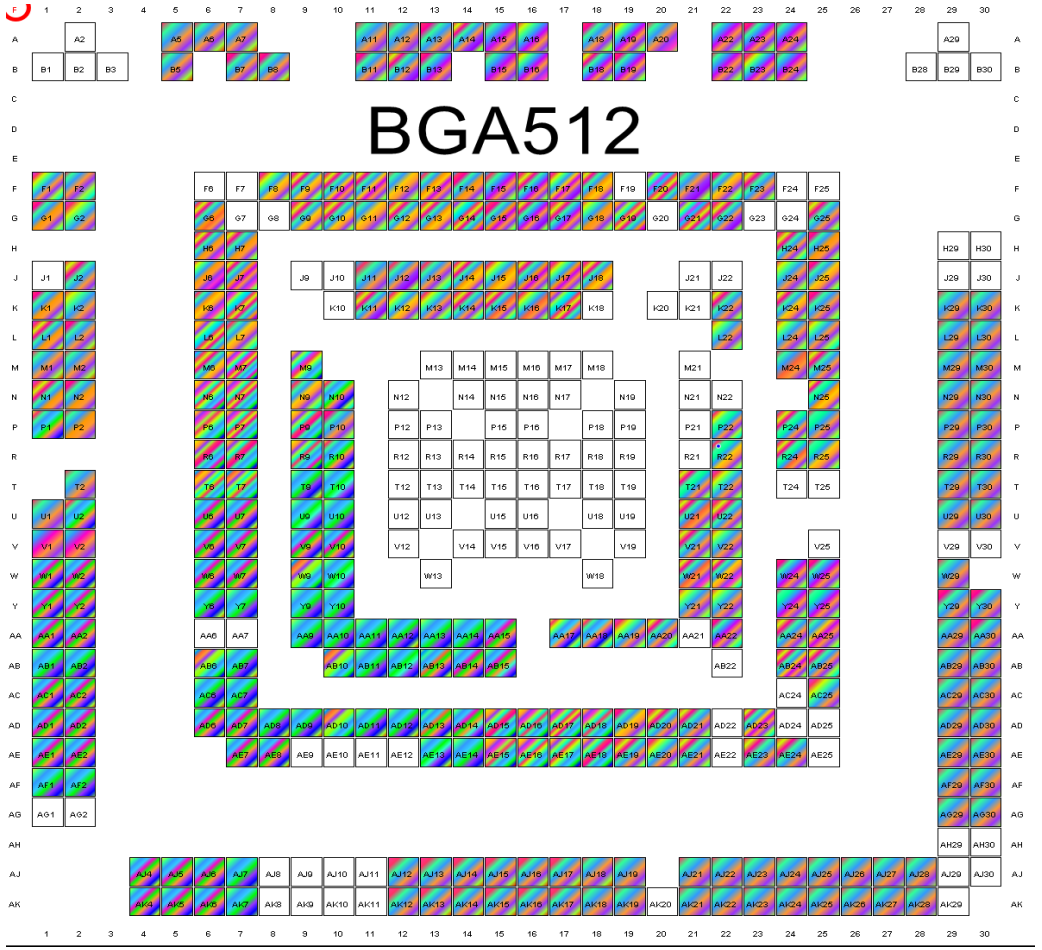
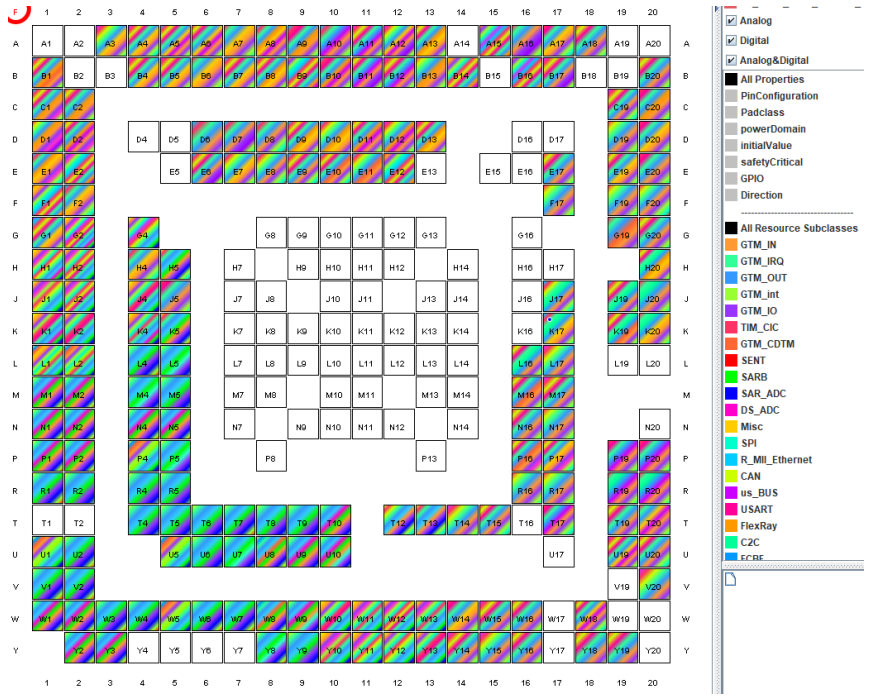
Common Family-µC Ball Out

BGA512



BGA292



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