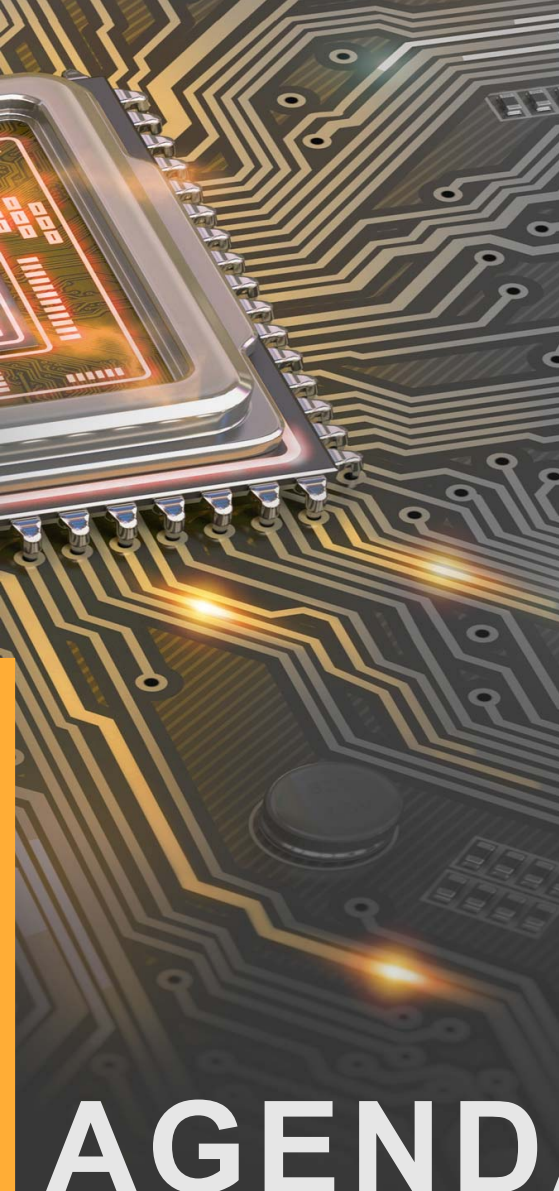


 **GTM** Tech Day 2022

TRACE32[®] Debug and Trace
Support for GTM

Elmar Stahleder Lauterbach GmbH Sep. 22./23. 2022





1. Debugging Scenarios
2. GTM V4.1, a big improvement for debugging
3. Onchip /Offchip Trace Features

AGENDA

Supported CPU Families with GTM



AURIX™ TriCore™ TC2xx, TC3xx and TC4x



MPC57xx Power Architecture®

Arm® Cortex®-R52, Cortex®-M33 based S32E2, S32Z2



RH850



SPC57xx, SPC58xx Power Architecture®

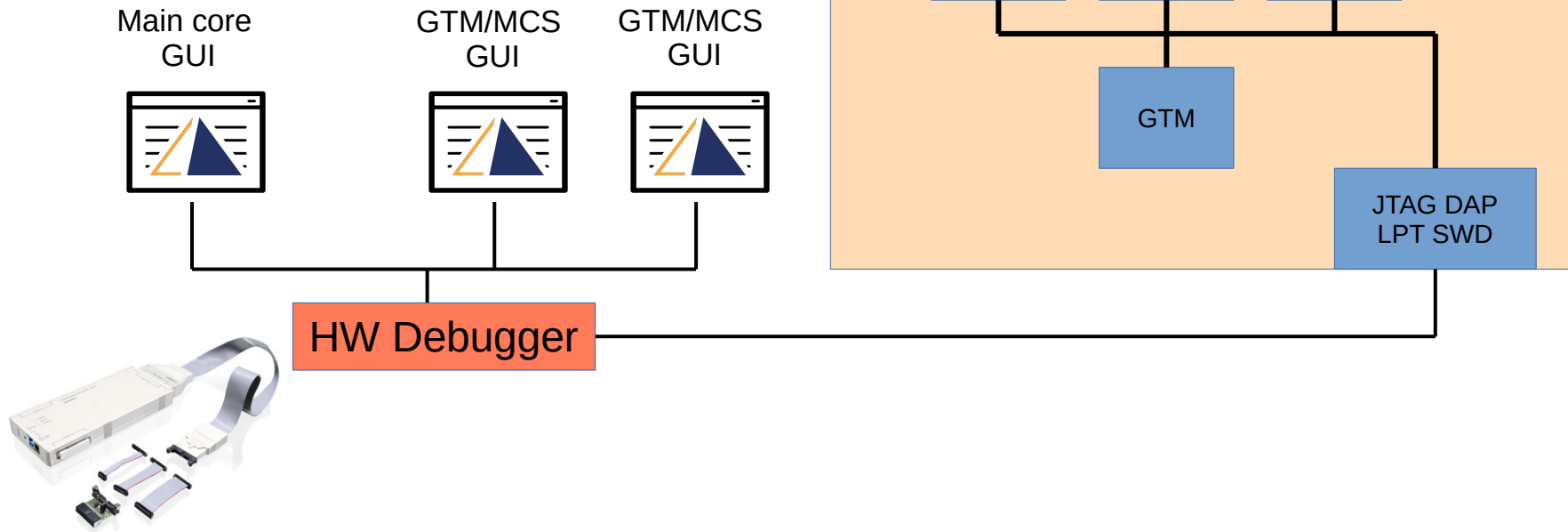
Arm® Cortex®-R52, Cortex®-M4 based

Stellar SR6P6/P7/G7

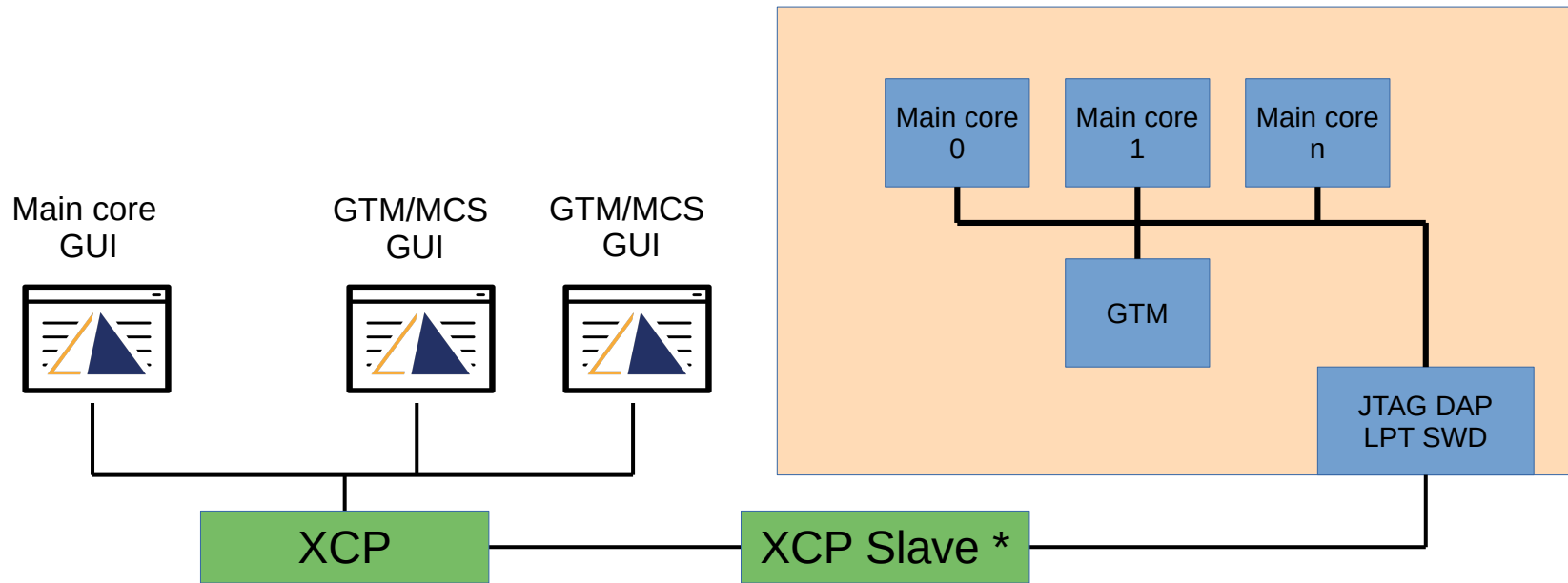


Debugging

The debugger for the main core e.g. TriCore™ already includes the license for GTM debugging



XCP Debugging



* e.g. Calibration Tool



Access a Virtual GTM

Main core
GUI



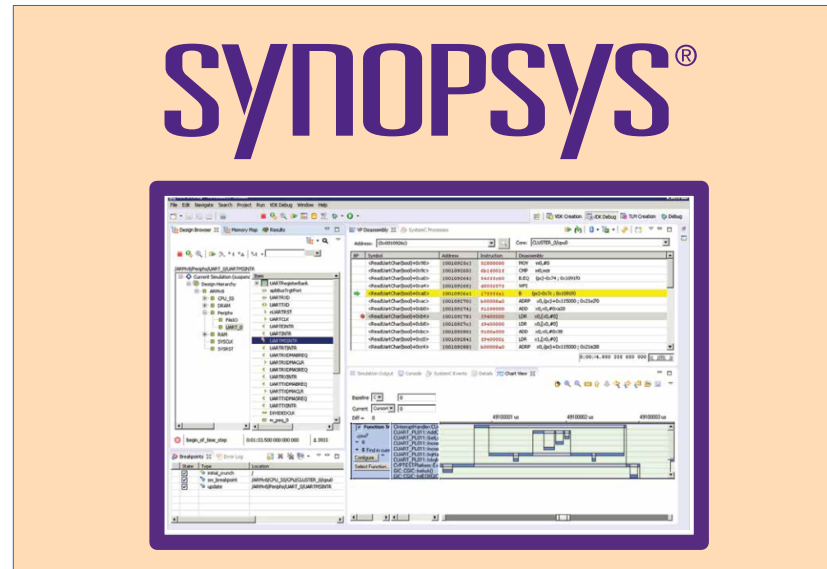
GTM/MCS
GUI



GTM/MCS
GUI



MCD API *



* MCD is an open interface, more details at https://www.lauterbach.com/mcd_api.html

Debug Features

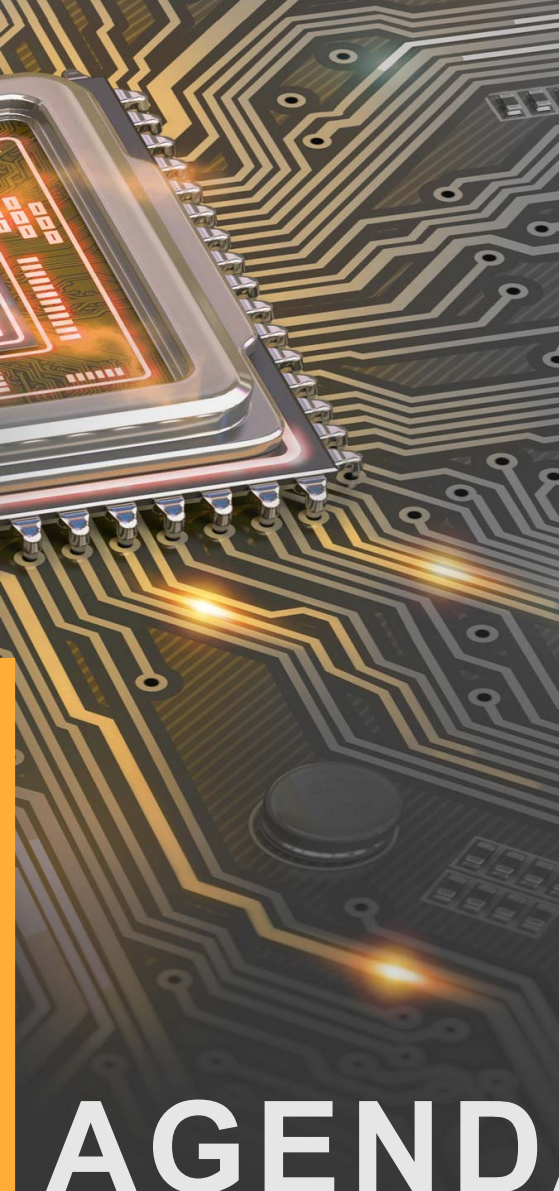
- Debug Support for MCS
- C Level Debugging
- Inline Assembler
- Peripheral View of GTM Registers, also when the Program Execution is Running
- Synchronous Go/Break between Main Core e.g. TriCore™ and GTM

The screenshot shows a debugger window titled "B::List.auto" displaying assembly code. The code is color-coded and includes C-level comments. The assembly instructions are: `andl r4,0xffff`, `movl r6,0xffff`, `wurmx r4,tbu_ts1`, `mov r4,r5`, `shl r4,2`, `mrdd r4,r4,0x4E8`, `mwr r4,0x538`, `movl r4,0x20`, `mov msint,r4`, `addl r5,0x1`, and `atsl r5,0x14`. The comments include `delay &= 0xffff;`, `__wurmx(&TBU_TS1, delay, 0xFFFF);`, `uiOutput = outputchain[i];`, `MSINT = 0x20;`, and `for (int i = 0; i < 20; i++) {`.

The screenshot shows a debugger window titled "B::CORE.List" displaying a table of core states. The table has columns for 'sel', 'core', 'stop', 'state', 'pc', and 'symbol'. The data is as follows:

sel	core	stop	state	pc	symbol
✓	0	◆		P:000002E4	\\mcs00\mcs00\main+0x24
	1	◆		P:0000005C	\\mcs00\mcs00\mainChannel1+0x3C
	2	◆		P:00000104	\\mcs00\mcs00\mainChannel2+0x3C
	3	◆		P:000001AC	\\mcs00\mcs00\mainChannel3+0x3C
	4	◆		P:00000254	\\mcs00\mcs00\mainChannel4+0x3C
	5	◆		P:00000014	\\mcs00\Global\mcstext.vector
	6	◆		P:00000018	\\mcs00\Global\mcstext.vector
	7	◆		P:0000001C	\\mcs00\Global\mcstext.vector





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Debugging before GTM V4.1

TC2xx TC3xx:

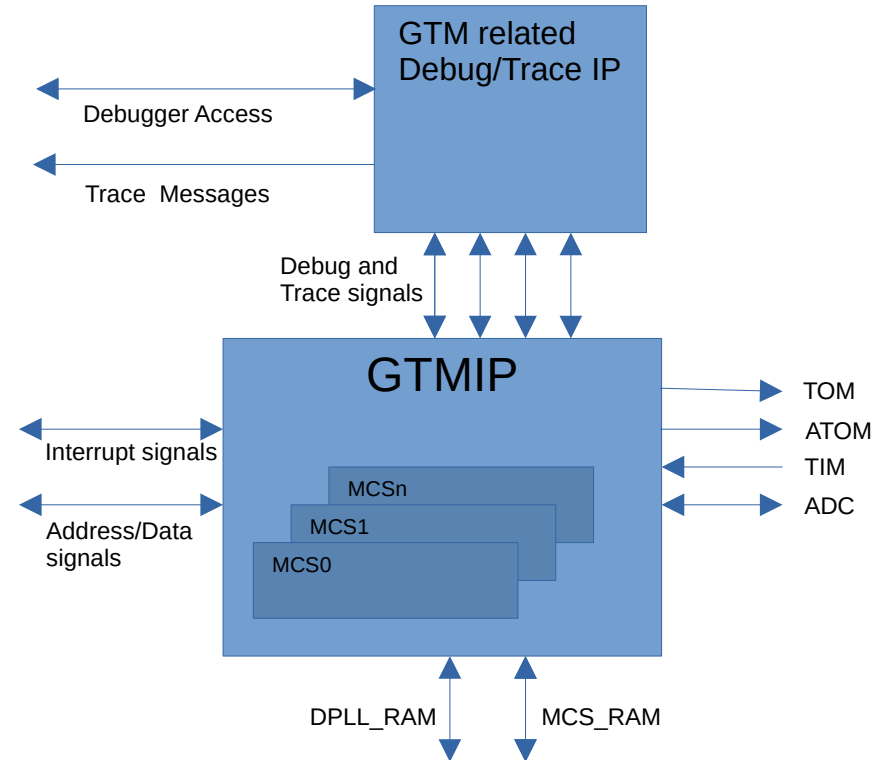
MCDS Multi-Core Debug Solution and
OTGM OCDS Trigger Mux

MPC57xx SPC57xx SPC58xx:

GTMDI GTM Development Interface

RH850:

TEU Trigger Event Unit



Debugging GTM V4.1

TC4x:

MCDS OTGM

GTM Hardware Breakpoints

SR6P7 S32E2 S32Z2:

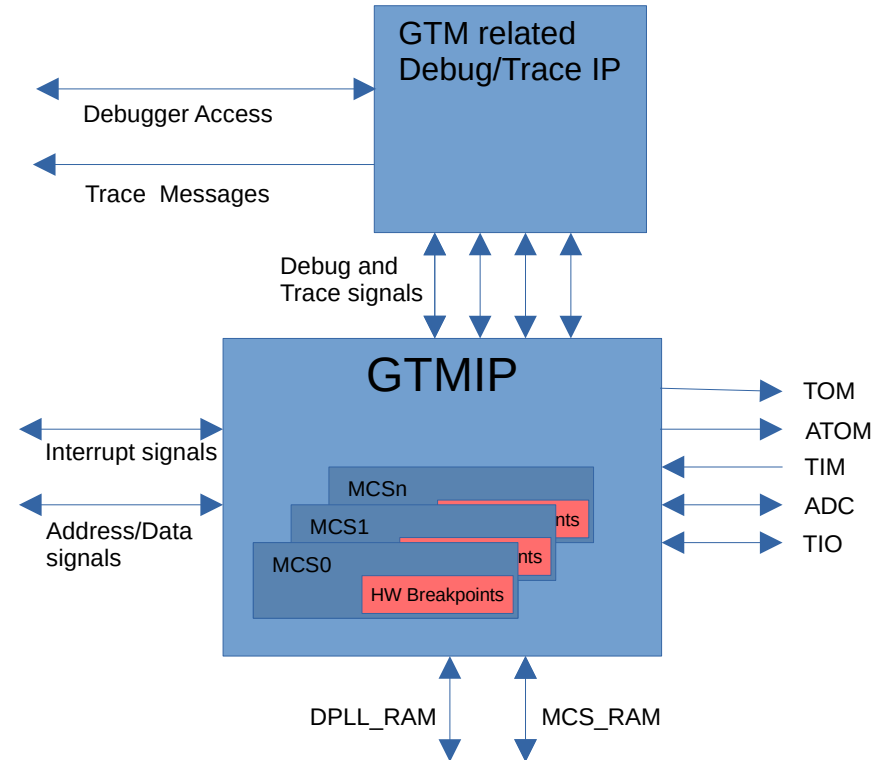
GTMDI

GTM Hardware Breakpoints

RH850 U2B:

TEU

GTM Hardware Breakpoints





Debug Features GTM V4.1

- New Hardware Breakpoint Unit
- Two Breakpoints (break before make) for every MCS Module
Used for Single Stepping or Breakpoints
- Breakpoints on Program Address or Range
- Breakpoints on Data Address or Range; Read or Write Access
- Breakpoint on Data Address or Range and Data Value
- Channel Selection possible

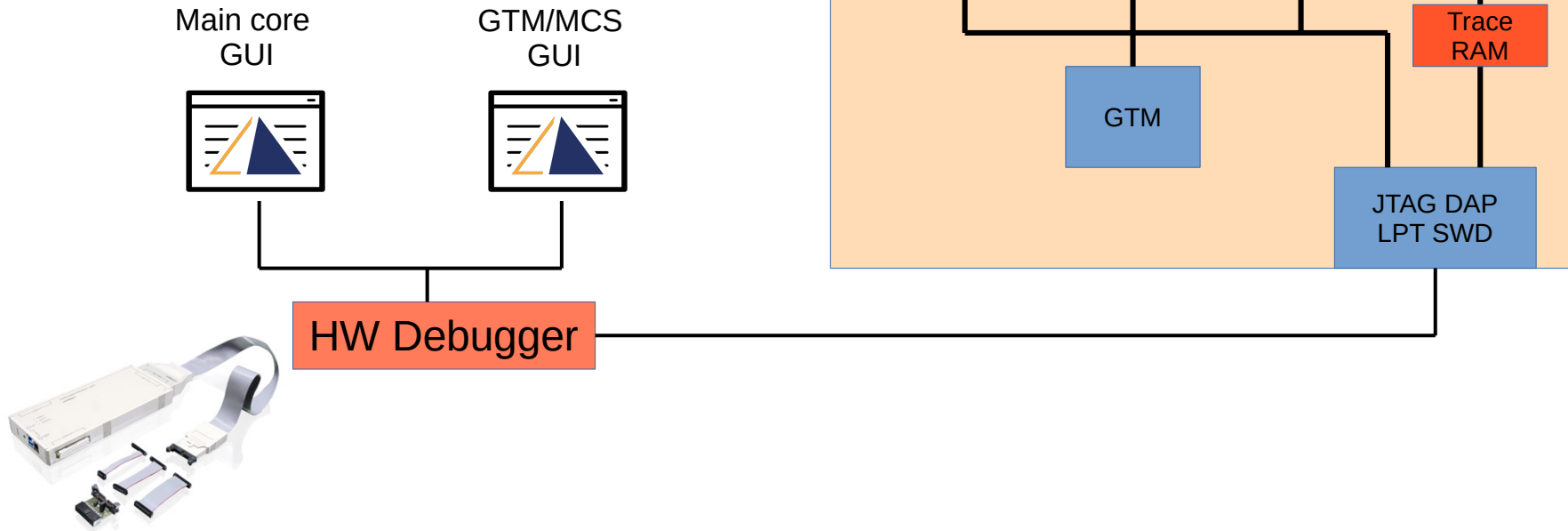


1. Debugging Scenarios
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Onchip Trace

The Trace License for the main core e.g. TriCore™ already includes the Trace License for GTM

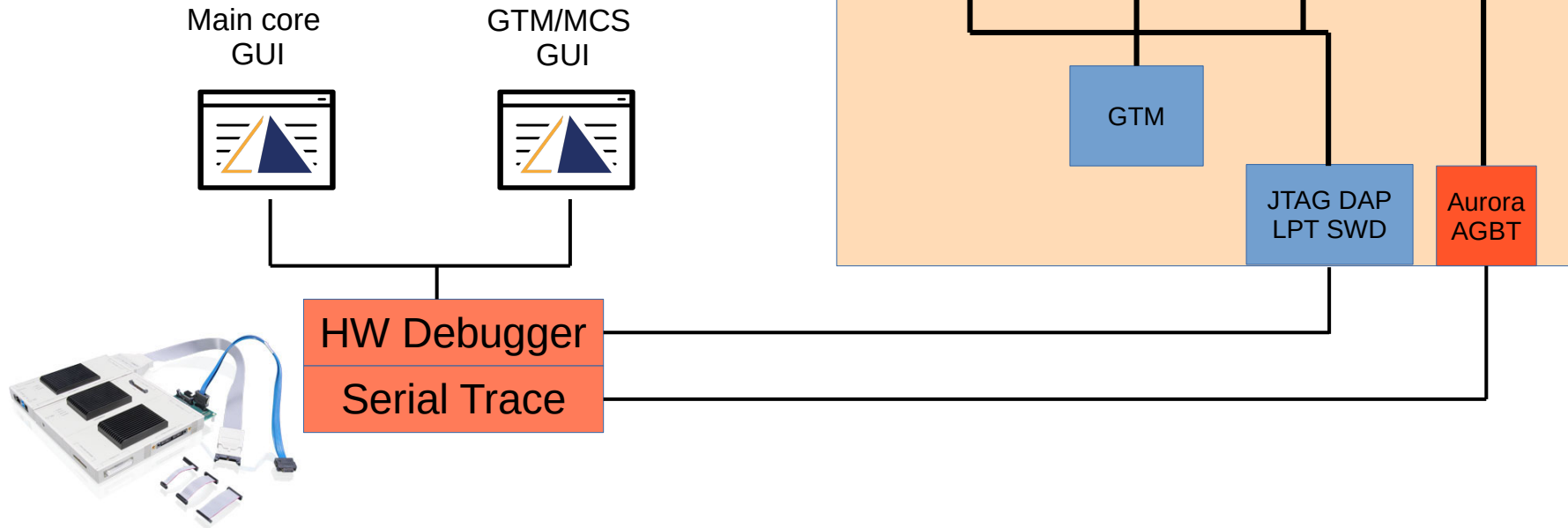


Off-Chip Trace

Aurora GigaBit Trace

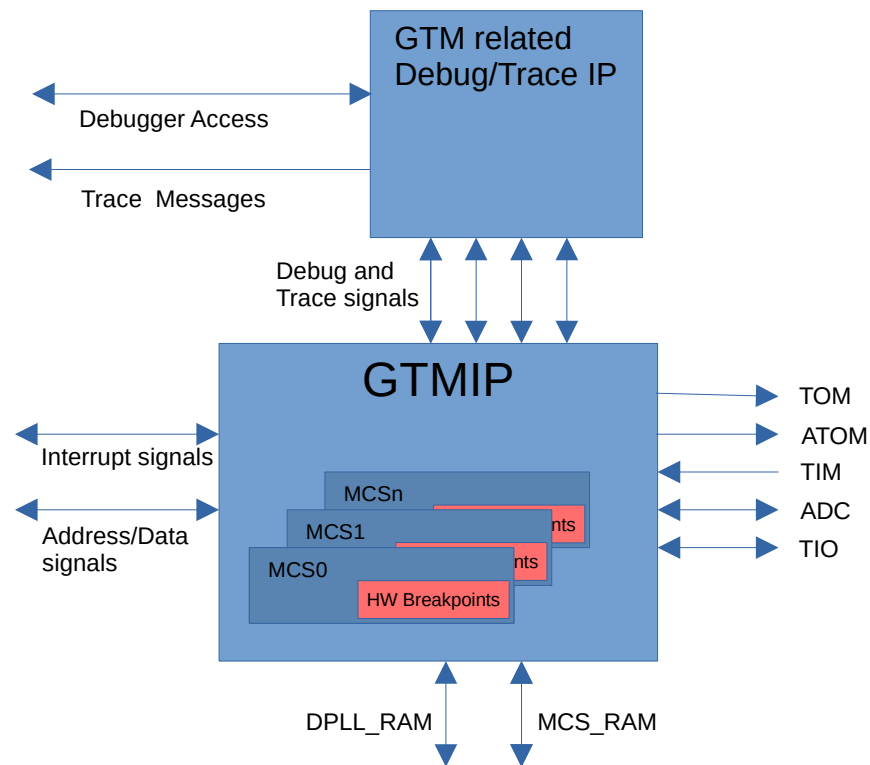
Current Chips Support:

- Up to 6.25 Gbit/s per Lane
- Up to 4 Lanes

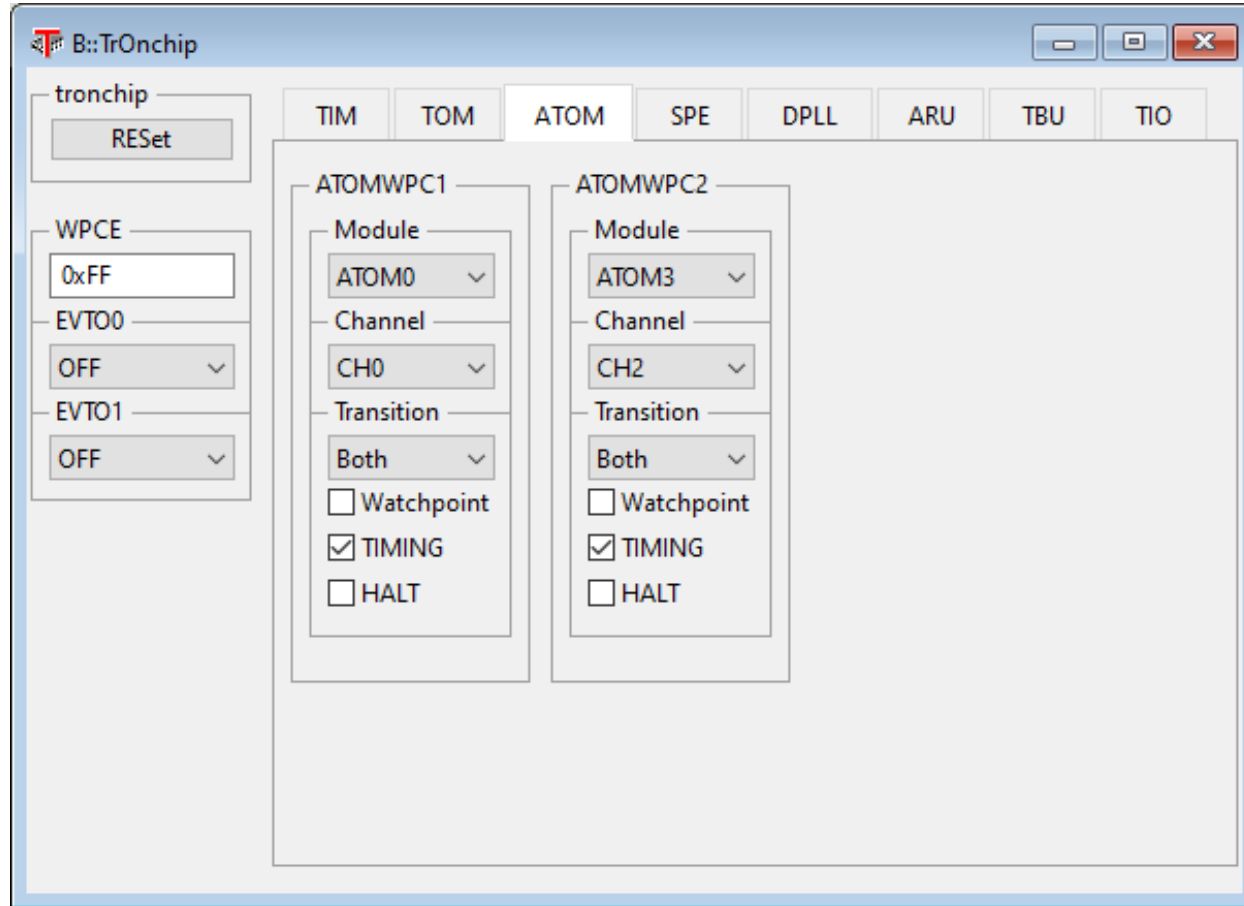


GTM Tracing

- Multi Channel Sequencer (MCS)
- Advanced Routing Unit (ARU)
- I/O Channels (TIM, TOM, ATOM and TIO)
- Digital PLL Module (DPLL)
- Sensor Pattern Evaluation (SPE)
- Time Base Unit (TBU)



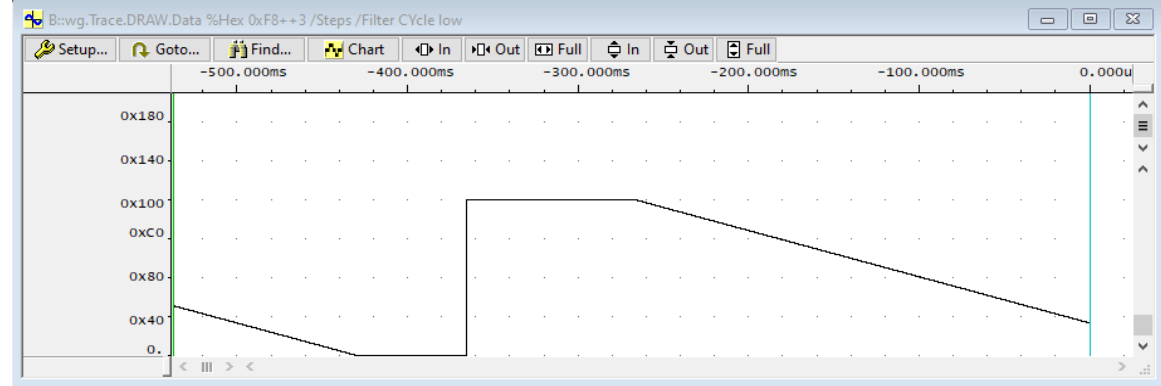
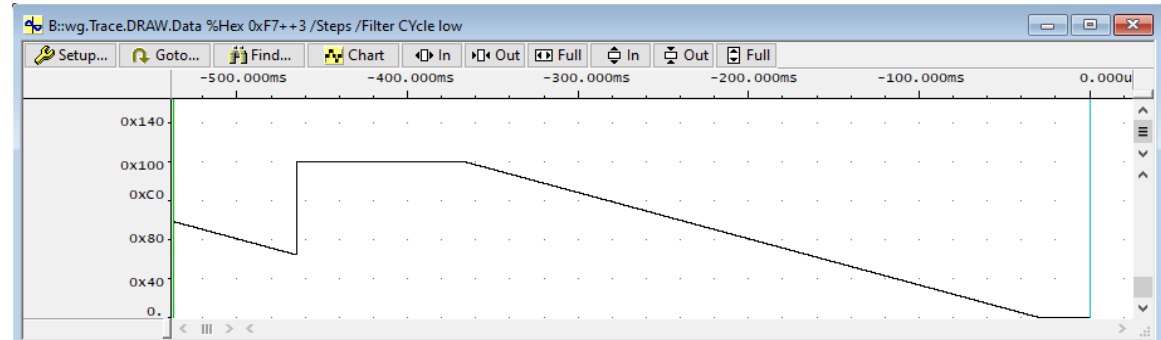
GTM Trace Sources



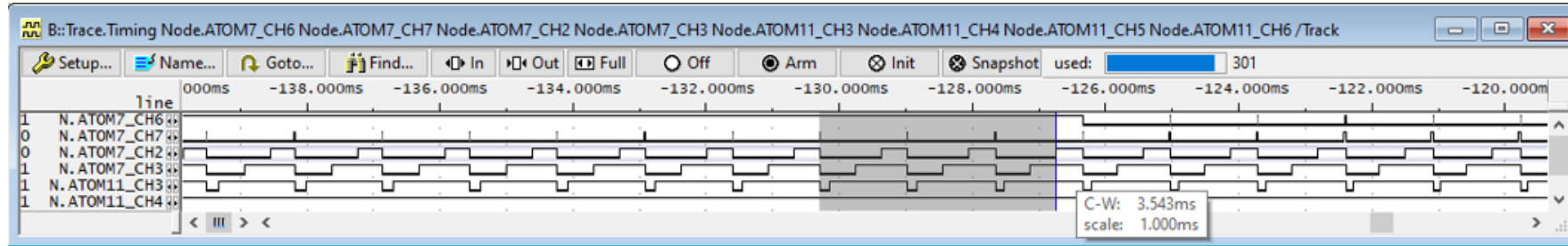
Advanced Routing Unit (ARU)



record	run	address	cycle	data	symbol	ti.back
-001140		ARU:000000F7	low	000000DC		0.020us
-001120		ARU:000000F8	high	00000100		2.580us
-001102		ARU:000000F8	low	00000090		0.020us
-001055		ARU:000000F7	high	00000100		1.313ms
-001036		ARU:000000F7	low	000000D8		0.020us
-001016		ARU:000000F8	high	00000100		2.580us
-000998		ARU:000000F8	low	0000008F		0.020us
-000951		ARU:000000F7	high	00000100		1.313ms
-000932		ARU:000000F7	low	000000DA		0.020us
-000912		ARU:000000F8	high	00000100		2.580us
-000894		ARU:000000F8	low	0000008E		0.020us
-000847		ARU:000000F7	high	00000100		1.313ms
-000828		ARU:000000F7	low	000000D9		0.020us
-000808		ARU:000000F8	high	00000100		2.580us
-000790		ARU:000000F8	low	0000008D		0.020us
-000743		ARU:000000F7	high	00000100		1.313ms
-000721		ARU:000000F7	low	000000D8		0.020us
-000702		ARU:000000F8	high	00000100		2.580us
-000683		ARU:000000F8	low	0000008C		0.020us
-000636		ARU:000000F7	high	00000100		1.313ms
-000617		ARU:000000F7	low	000000D7		0.020us
-000598		ARU:000000F8	high	00000100		2.580us
-000579		ARU:000000F8	low	00000088		0.020us
-000531		ARU:000000F7	high	00000100		1.313ms
-000512		ARU:000000F7	low	000000D6		0.020us
-000492		ARU:000000F8	high	00000100		2.580us
-000474		ARU:000000F8	low	0000008A		0.020us
-000427		ARU:000000F7	high	00000100		1.313ms
-000408		ARU:000000F7	low	000000D5		0.020us
-000388		ARU:000000F8	high	00000100		2.580us
-000370		ARU:000000F8	low	00000089		0.020us
-000323		ARU:000000F7	high	00000100		1.313ms
-000304		ARU:000000F7	low	000000D4		0.020us
-000284		ARU:000000F8	high	00000100		2.580us
-000266		ARU:000000F8	low	00000088		0.020us
-000219		ARU:000000F7	high	00000100		1.313ms
-000200		ARU:000000F7	low	000000D3		0.020us
-000180		ARU:000000F8	high	00000100		2.580us
-000156		ARU:000000F8	low	00000087		0.020us
-000105		ARU:000000F7	high	00000100		1.313ms
-000083		ARU:000000F7	low	000000D2		0.020us
-000064		ARU:000000F8	high	00000100		2.580us
-000045		ARU:000000F8	low	00000086		0.020us



I/O Channels (TIM, TOM, ATOM and TIO)



Logic analyzer measurement window for N.ATOM7_CH2, showing statistics for 394 records over a 12.621ms interval.

	avr	min	max	bits & jitter
time	853.240us	832.680us	873.800us	
time lead	460.030us	436.900us	483.160us	
time tail	1.316ms	1.316ms	1.316ms	438.552us
frequency	759.Hz	759.Hz	759.Hz	2.28KHz
duty cycle	65:35	63:37	67:33	7.618%

Logic analyzer like measurements





Thank You!