Implementing serial automotive communication protocols with the Bosch GTM-IP

CISC Semiconductor Corp. – Mountain View (CA), U.S.A.

Detroit, October 10-11, 2017

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- CISC delivers worldwide both products and engineering services to our customers being represented in the Semiconductor, Automotive, Wireless Communication and RFID/NFC industry.

*) **System** = heterogeneous networked embedded microelectronic systems

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- 100% of R&D staff hold at least a master degree

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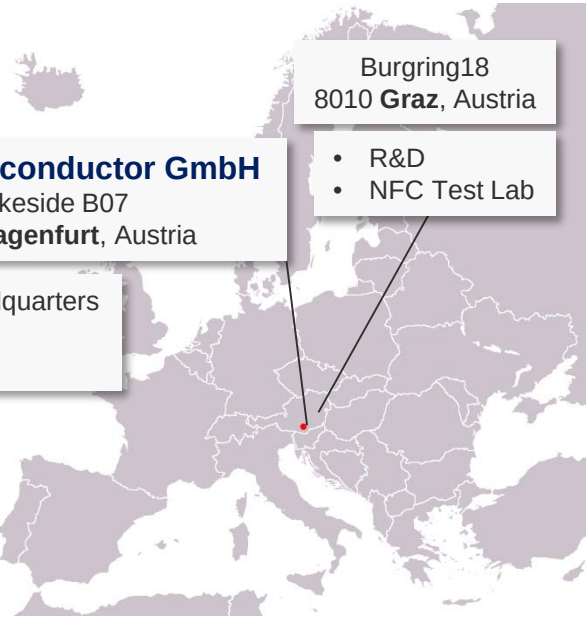

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AT Automotive

- Electrical Power Train
- Safety Systems
- Body electronics
- Transceiver
  - FlexRay
  - CAN
  - LIN
- Advanced µC's
  - TRICORE verification
  - BOSCH GTM IP

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  - 13,56 MHz
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- Methodology
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  - Embedded system simulation
  - Design Centering / Yield Optimization

Agenda

- Characteristics of serial protocols
- GTM features suitable for serial protocols
- Concepts for implementation
  - low level; and
  - Protocol level
- Verification
  - Model/Testbench
  - On FPGA
  - Compliance to standards (e.g. AUTOSAR)
- CPU interfacing
- Examples

Characteristics of serial protocols

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Challenges

- Synchronization
- Data rate detection
- Bus arbitration
- High clock variations (e.g. +/-20 % for SENT)
- Allowed deviation between successive calibration pulses very low (e.g. +/-1.5625 % for SENT)
- Error recovery

Concepts for implementation

- All protocol features covered by the MCS
  - Minimize workload for the CPU
  - CPU just configures the GTM modules
- Message handling
  - Using different interfaces between CPU und MCS according to message priorities

GTM features suitable for serial protocols

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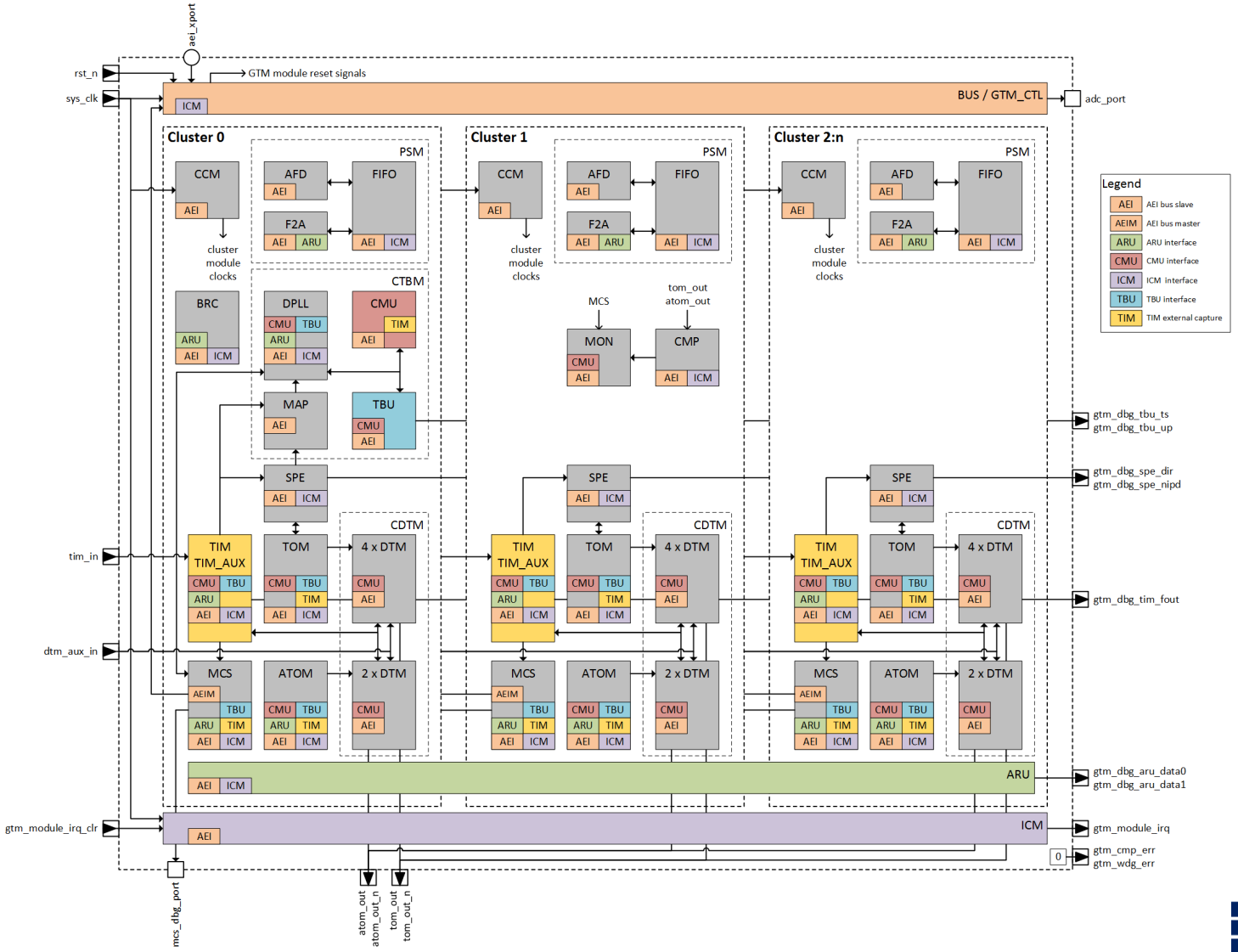
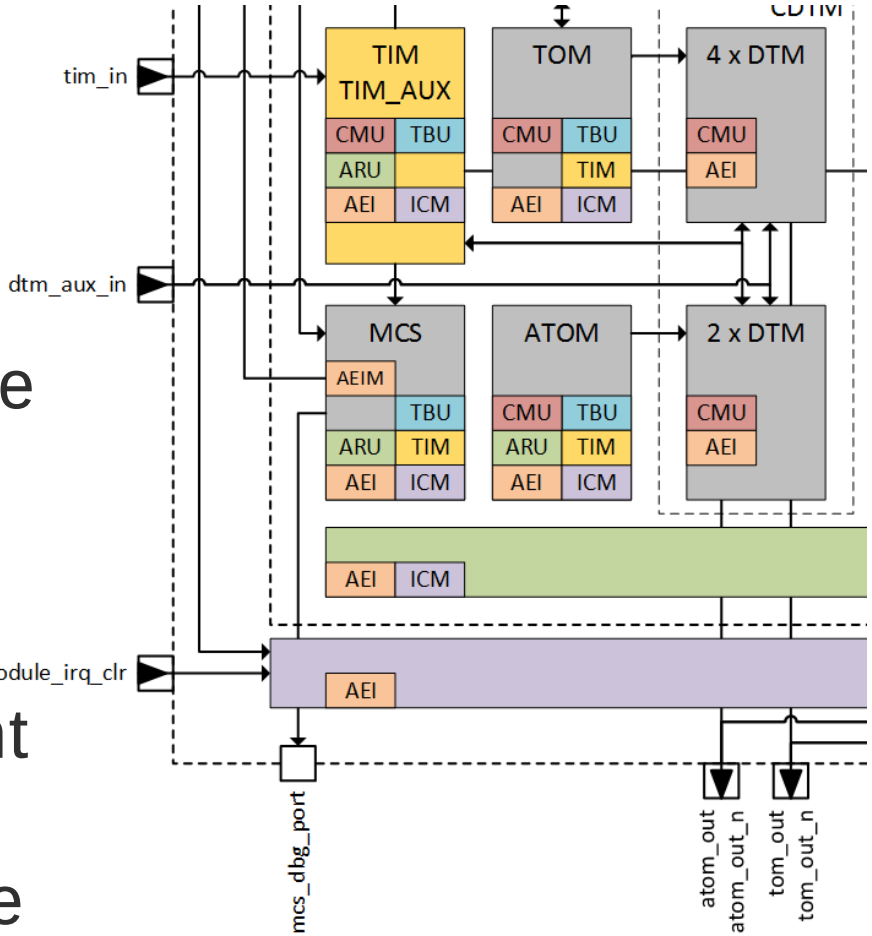
GTM V3.1 overview



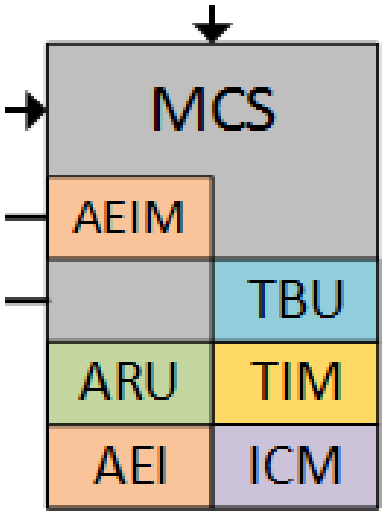
GTM units in use

- MCS - Multi Channel Sequencer
- ARU - Advanced Routing Unit
- TIM - Timer Input Module
- ATOM - ARU-connected Timer Output Module
- TBU - Time Base Unit
- CMU - Clock Management Unit
- DTM - Dead Time Module



MCS and serial protocols

- MCS – Multi Channel Sequencer
  - CPU-independent data processing
  - Input data from TIM (RX)
  - Output data via ATOM (TX)
  - Timing with TBU
  - ARU connected
  - AEI-BUS master and slave

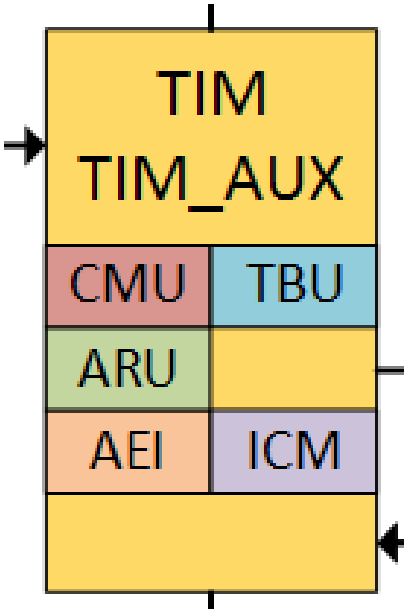


ARU and serial protocols

- ARU – Advanced Routing Unit
  - CPU-independent data exchange between GTM submodules
  - Resource efficient
  - Configurable streams between data sources and data destinations
  - Deterministic round trip time via round-robin arbitration

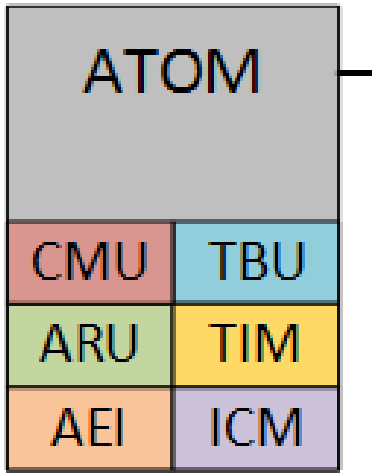
TIM and serial protocols

- TIM – Timer Input Module
  - Input signal filtering and characterization
  - Flexible input selection
  - Timestamps via TBU
  - Duration via CMU
  - Various operation modes possible through flexible channel architecture
  - ARU connected



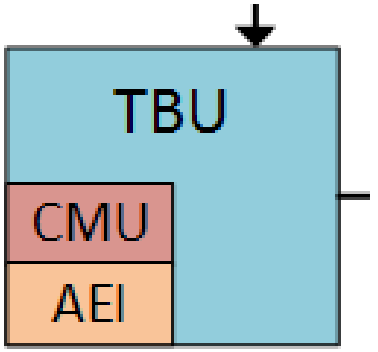
ATOM and serial protocols

- ATOM – ARU-connected Timer Output Module
  - Complex output signal generation
  - CPU-independent (ARU connected)
  - Various operation modes possible through flexible channel architecture
  - Global trigger mechanism
  - Flexible timings via CMU
  - Serial output signal through internal shift register mode (“Signal output mode serial” – SOMS)



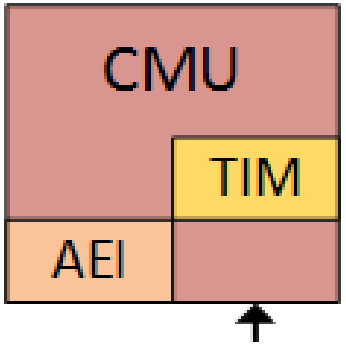
TBU and serial protocols

- TBU – Time Base Unit
  - Global time base for GTM submodules
  - Up to 4 independent channels
  - 2 channels with forward/backward counter modes (e.g. angle clocks)
  - 1 channel with modulo counter mode



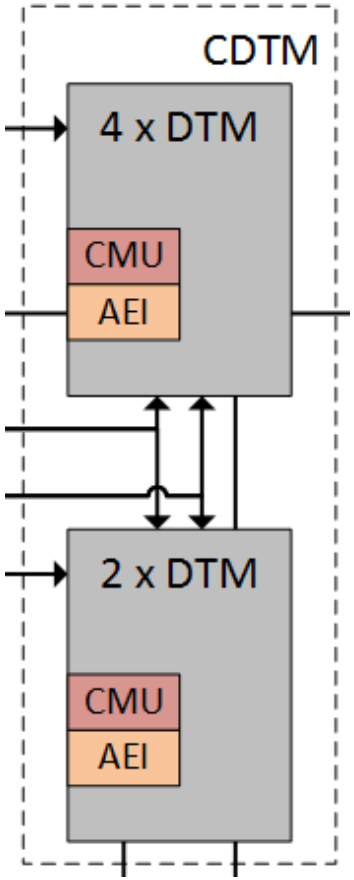
CMU and serial protocols

- CMU – Clock Management Unit
  - Clock generation for GTM counters
  - Global fractional divider
  - Configurable clock lines with freely programmable clock prescaler
  - Non-configurable clock lines
  - External clock lines



DTM and serial protocols

- DTM – Dead Time Module
  - Enhanced signal routing



Verification

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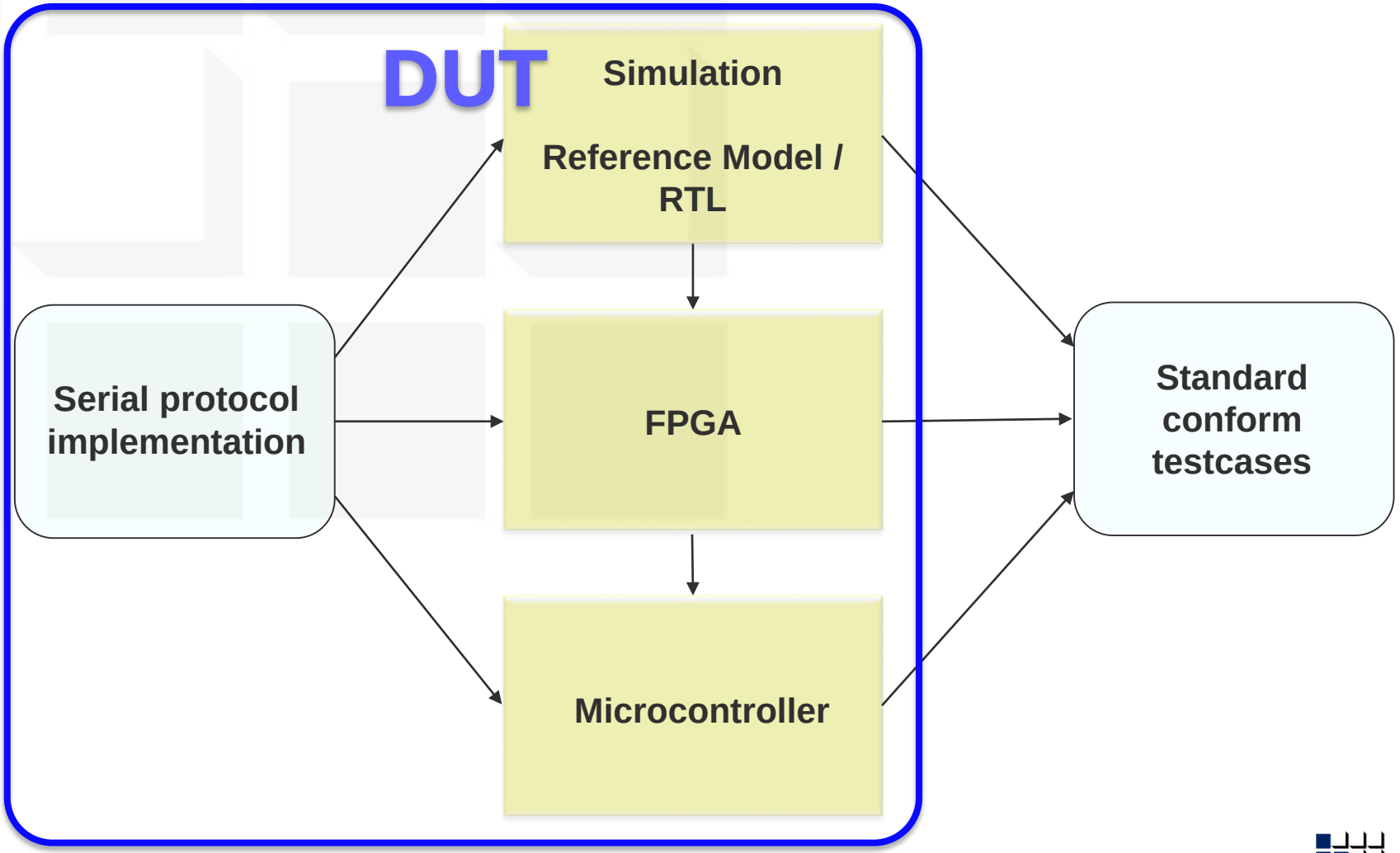
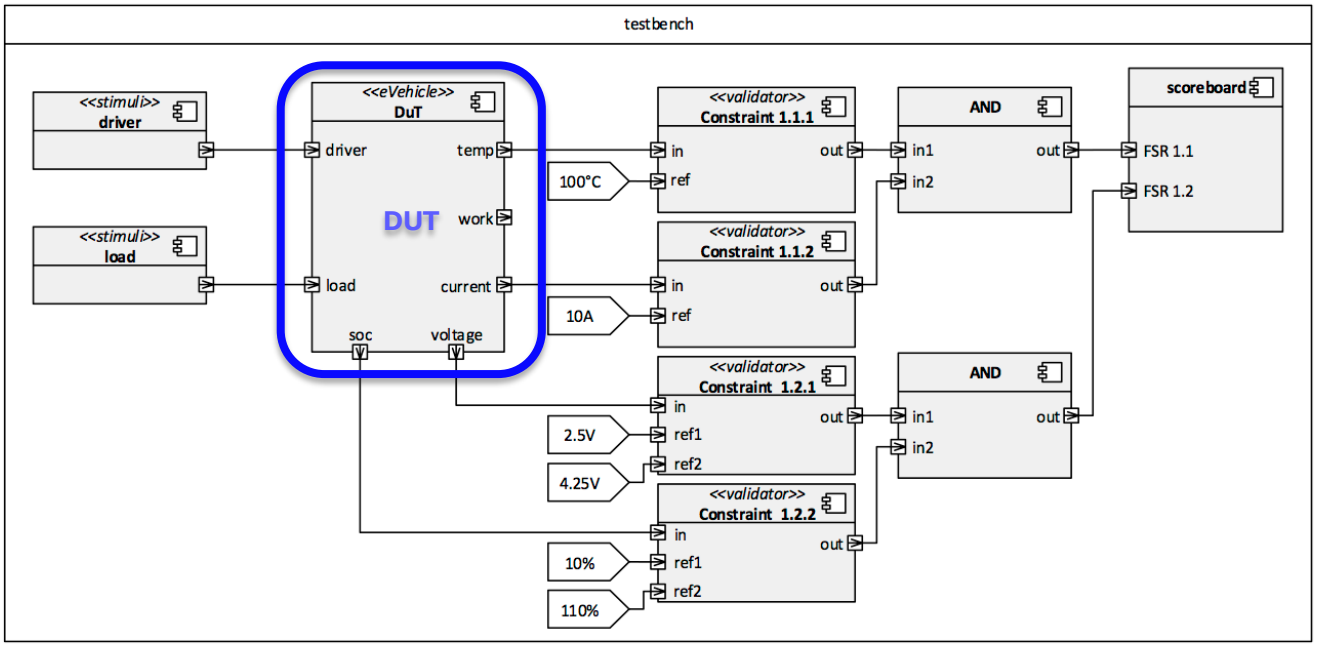
Test procedure flow



Test procedure flow

- Test bench derived from e.g. safety requirements and constraints
- Constrained Random Verification (CRV) with UVM (run Monte Carlo)



CISC SHARC®

Eclipse based simulation and verification environment

µContoller interfacing

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MCU interfacing concepts

- Configuration of the MCS program
  - Variables in the MCS memory
- Data exchange between MCS and CPU
  - MCS memory
    - DMA access by the CPU
    - Interrupt generated by MCS if new data is available
  - ARU via FIFO
    - Fill level based interrupt

Examples

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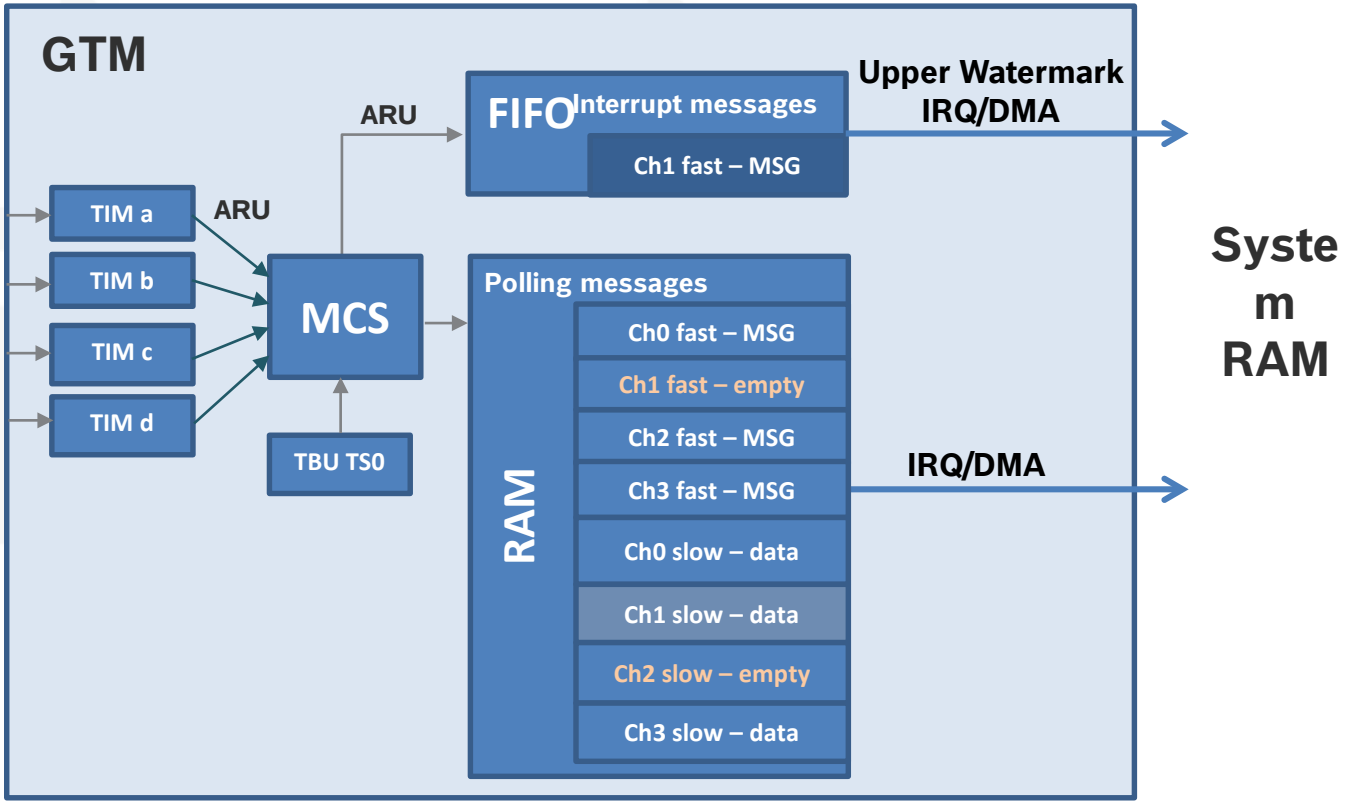
SENT implementation



SENT features

based on GTM V1.5

- Up to 4 parallel SENT channels using 1 MCS
- 3 µs clock tick
- Fast/Slow channel reception
- FIFO for interrupt messages
- RAM for polling messages
- Message diagnostics completely done by MCS

LIN implementation

based on GTM V1.5

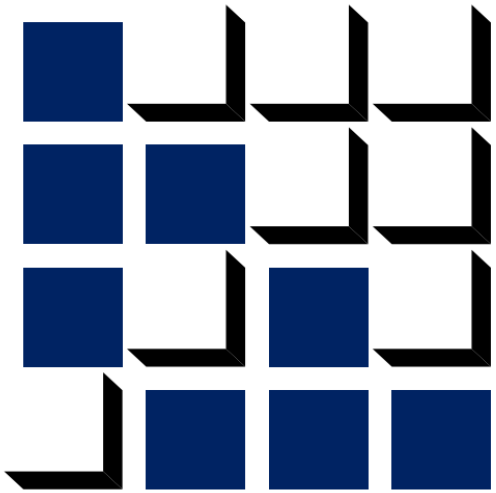
- LIN master
- 20 kbit/s
- 1 ATOM, 1 MCS, 1 TIM per LIN master
- CRC check done by the MCS

CAN implementation

based on GTM V3.1

- Classical CAN
- 2 cluster/CAN -> max 6 CAN nodes
- Synchronization using GTM building blocks
- Message prioritization
- Acceptance filtering
- Error detection and handling in MCS

- Feasibility study for 500 kbit/s



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